an n-channel field effect transistor and a p-channel field effect transistor in the CMOS circuit;

said n-channel field effect transistor comprising:

a crystalline semiconductor formed on an insulating surface;

a source region, a drain region and a channel forming region in the crystalline semiconductor;

a gate insulating film;

a gate electrode formed over the channel forming region;

said channel forming region comprising:

a plurality of carrier moving regions;

a plurality of impurity regions,

C1 Cont

wherein the plurality of impurity region of the channel forming region are formed locally for pinning of a depletion layer,

wherein the depletion layer is formed from the drain region toward the channel forming region and the source region,

wherein each of the impurity regions comprises an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

19. (Amended) An integrated circuit comprising:

a memory circuit;

a field effect transistor in the memory circuit;

said field effect transistor comprising:

a crystalline semiconductor;

a source region, a drain region and a channel forming region in the crystalline semiconductor;

a gate insulating film;

a gate electrode formed over the channel forming region;

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said channel forming region comprising:

a plurality of carrier moving regions;

a plurality of impurity regions;

wherein the plurality of the impurity region in the channel forming region are formed locally for pinning of a depletion layer,

wherein the depletion layer is formed from the drain region toward the channel forming region and the source region,

wherein each of the impurity regions comprises an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

20. (Amended) An integrated circuit according to claim 18,

wherein the impurity element is for forming a built-in potential difference locally in the channel forming region.

23. (Amended) An integrated circuit according to claim 18, wherein the impurity element belongs to group XV.

25. (Amended) An integrated circuit according to claim 18, wherein the carrier moving regions are intrinsic or substantially intrinsic.

28. (Amended) An integrated circuit according to claim 18, wherein a width W of the channel forming region, a total width W_{pi} of the impurity regions, and a total width W_{pa} of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

29. (Amended) An integrated circuit according to claim 18, wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

30. (Amended) An integrated circuit according to claim 18,

wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

31. (Amended) An integrated circuit according to claim 18,

wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

C4 cont

32. (Amended) An integrated circuit according to claim 18,

wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

33. (Amended) An integrated circuit according to claim 18,

wherein the impurity regions have dot patterns.

34. (Amended) An integrated circuit according to claim 18,

wherein the impurity regions have linear patterns substantially parallel with a channel direction.

35. (Amended) An integrated circuit according to claim 18,

wherein a threshold voltage is controlled by controlling widths of the carrier moving regions.

36. (Amended) An integrated circuit according to claim 18, wherein the impurity element in the impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/cm^3.

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37. (Amended) The integrated circuit of claim 18 in combination with at least an electric apparatus selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

Please add new claims 41-56.

--41. (New) An integrated circuit according to claim 19, wherein the impurity element is for forming a built-in potential difference locally in the channel forming region.

42. (New) An integrated circuit according to claim 19, wherein the impurity element belongs to group XV.

43. (New) An integrated circuit according to claim 42, wherein the impurity element is phosphorus or arsenic.

44. (New) An integrated circuit according to claim 19, wherein the carrier moving regions are intrinsic or substantially intrinsic.

45. (New) An integrated circuit according to claim 44, wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than 5×10^{15} atoms/cm^3 and an oxygen concentration is less than 2×10^{18} atoms/cm^3.

46. (New) An integrated circuit according to claim 44, wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than 5×10^{15} atoms/cm^3 and an oxygen concentration is less than 1×10^{17} atoms/cm^3.

47. (New) An integrated circuit according to claim 19, wherein a width W of the channel forming region, a total width W_{pi} of the impurity regions, and a total width W_{pa} of

regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

48. (New) An integrated circuit according to claim 19, wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

49. (New) An integrated circuit according to claim 19, wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

50. (New) An integrated circuit according to claim 19, wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

51. (New) An integrated circuit according to claim 19, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

52. (New) An integrated circuit according to claim 19, wherein the impurity regions have dot patterns.

53. (New) An integrated circuit according to claim 19, wherein the impurity regions have linear patterns substantially parallel with a channel direction.

54. (New) An integrated circuit according to claim 19, wherein a threshold voltage is controlled by controlling widths of the carrier moving regions.

55. (New) An integrated circuit according to claim 19, wherein the impurity element in the impurity regions is at a concentration of 1×10^{17} to 1×10^{20} atoms/cm^3.

56. (New) The integrated circuit of claim 19 in combination with at least an electric apparatus selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal ~~computer,~~ a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.--